

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

sub 4  
B2  
Claim 1 (currently amended): A method for determining location of a short in a circuit, comprising the steps of :

(a) running a connectivity extract tool on an artwork of the circuit;  
(b) determining if a short exists in the circuit, wherein if a short exists the method comprises:

running a short locator tool, comprising

examining a schematic of the circuit,

creating a copy of the artwork of the circuit, and

inferring labels to the copy of the artwork; and

(c) comparing the artwork of the circuit to a schematic of the circuit.

Claim 2 (cancelled).

Claim 3 (original): The method of claim 2 where in the step of examining further comprises the step of evaluating a connectivity text file of the schematic.

Claim 4 (original): The method of claim 3 wherein the step of evaluating further comprises obtaining electrical connection information for each component.

Claim 5 (original): The method of claim 2 wherein the step of inferring further comprises the step of renaming signal names.

Claim 6 (original): The method of claim 2 further comprising the step of running the connectivity extract tool on the copy of the artwork.

Claim 7 (original): The method of claim 6 further comprising obtaining shortest path between conflicting labels in the circuit.

Claim 8 (original): The method of claim 7 further comprising modifying artwork of the circuit.

Claim 9 (original): The method of claim 8 further comprising running the connectivity extract tool on the modified artwork.

Claim 10 (original): A method for determining shortest path for a short in a circuit comprising the steps of:

examining a schematic of the circuit;

creating a copy of the artwork of the circuit, and  
inferring labels to the copy of the artwork.

Claim 11 (original): The method of claim 10 where in the step of examining further comprises the step of evaluating a connectivity text file of the schematic.

Claim 12 (original): The method of claim 11 wherein the step of evaluating further comprises obtaining electrical connection information for each component in the circuit.

Claim 13 (original): The method of claim 10 wherein the step of inferring further comprises the step of renaming common connection signal names.

Claim 14 (original): The method of claim 10 further comprising the step of running a connectivity extract tool on the copy of the artwork.

Claim 15 (original): The method of claim 14 further comprising obtaining shortest path between conflicting labels in the circuit.

Claim 16 (original): The method of claim 15 further comprising modifying artwork of the circuit.

Claim 17 (original): The method of claim 16 further comprising running the connectivity extract tool on the modified artwork.

Claim 18 (cancelled).